Digital Circuits Theory - Laboratory						
Academic year	Laboratory exercises on	Mode of studies	Field of studies	Supervisor	Group	Section
2020/2021	Wednesday 16:30 – 18:15	SSI	Informatics	KP	1	3

Report from Exercise No 3

Performed on: 14.10.2020

Exercise Topic: Bistable devices

Performed by:

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Purpose of the exercises

The aim of the tasks was to get to know the Flip-Flops – how they work and how to use them. It boiled down mainly to analyzing available flip-flops and describing them.

1 Description of the first task

Task 2

Recognise the triggering way of the synchronous D flip-flops (gated latch, master slave with or without 1s and 0s catching, or positive or negative edge-triggered). Draw timing charts used to resolve the problem.

1.1 Timing Chart

The only available flip-flop on my stand was D flip-flop. After plugging it in and testing, I got the following timing chart:

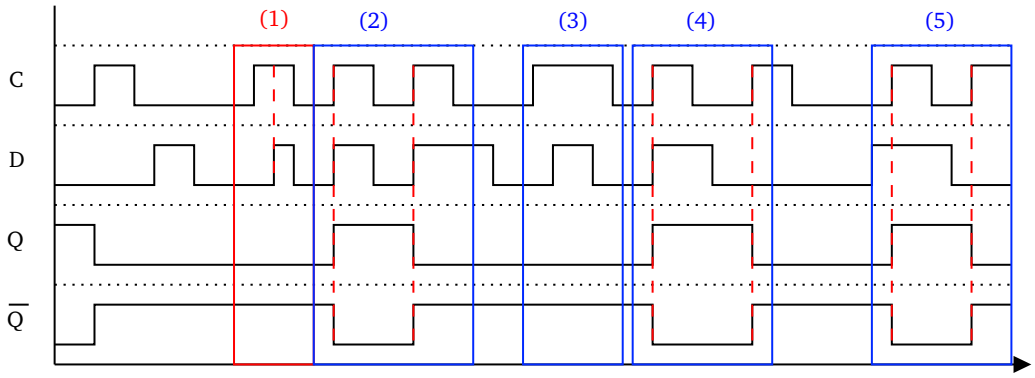

Figure 1: Timing Chart created during laboratory

(1) A change in the middle of the high state of the clock has no effect.

(2) Activating both the clock and D leads to a change of state. It is worth noting that this happens only for the positive edge, and no longer for the negative edge.

(3) The digital circuit does not notice the change of D inside the high state of the clock. There is also no gated latch or 1s and 0s catching.

(4) Again, activating D and the clock at the same time changes the state, but then activating the clock for low state D also changes the state of the output.

(5) Finally, we can see that the changes are only noticeable on the positive edge of the clock – in the enclosed example, the clock notices a change of state D and changes the state on the output. It does the same thing moments later for a low state D.

1.2 Excitation Table

D	$Q^t \rightarrow Q^{t+1}$
0	$0 \rightarrow 0$
1	$0 \rightarrow 1$
0	$1 \rightarrow 0$
1	$1 \rightarrow 1$

Table 1: Excitation Table of D flip flop

The resulting timing chart clearly indicates that the flip-flop works according to the excitation table – and therefore works properly.

1.3 Answer

From the given timing chart I determined that the flip-flop is triggered by a positive edge. The change of the output signal occurs only when the corresponding D signal is changed from zero to one.

2 Description of the second task

Task 3

Use only asynchronous inputs of the synchronous D flip-flop to determine their active value and which of them is dominant. Draw timing charts used to resolve the problem

2.1 Timing Chart

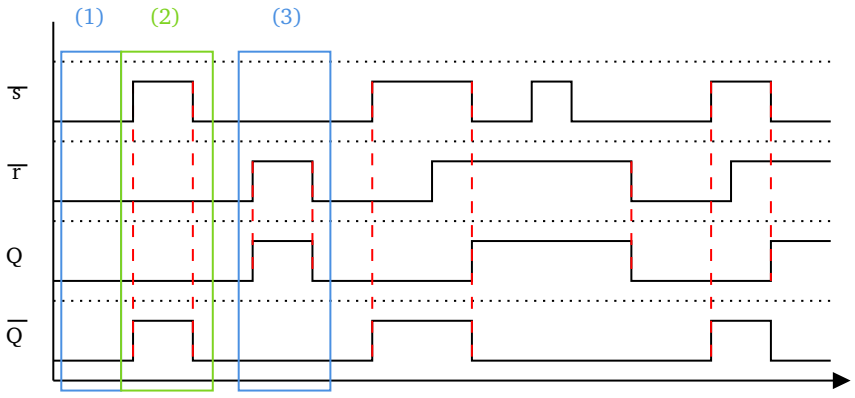

Figure 2: Timing Chart created during laboratory

(1) Zeros on both inputs lead to zeroes on both Q and $\overline{Q}$ inputs.

(2) If the state is high on $\overline{s}$ and low on $\overline{r}$, the output is high on $\overline{Q}$ and low on Q.

(3) A low on $\overline{s}$ and a high on $\overline{r}$ results in a high output on Q and a low on $\overline{Q}$.

2.2 Answer

We know that the reset is dominant, because for a high state $\overline{s}$ and a high state $\overline{r}$ the output Q gives zero. Their active values are zeroes.

3 Description of the third task

Task 5

For a flip-flop constructed as cross-coupled NANDs draw a timing chart illustrating the behaviour of the device. Basing on the chart determine the dominant input and the active level of both inputs.

3.1 The circuit

I started by connecting a digital circuit on my machine (see Fig 3).

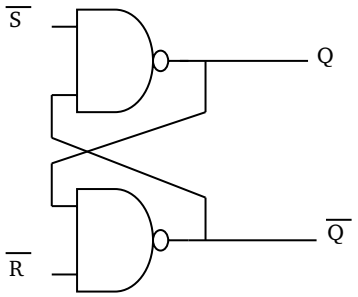

Figure 3: Cross-coupled NAND

After connecting the digital circuit I went to tests to create a timing chart.

3.2 Timing Chart

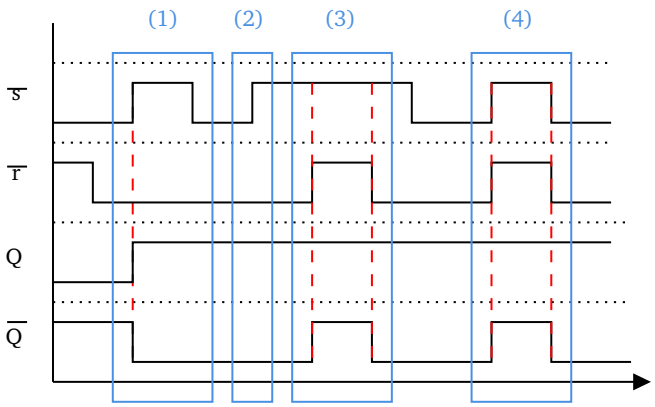

Figure 4: Timing Chart created during laboratory

(1) We can see that the high state of the input $\overline{s}$ made the output Q to change to 1 and $\overline{Q}$ to 0.

(2) Reactivating the input $\overline{s}$ does not affect the output.

(3) Enabling the input $\overline{r}$ during a high state of $\overline{s}$ has set $\overline{Q}$ to high state.

(4) Setting the inputs $\overline{s}$ and $\overline{r}$ to high again leads to high Q and $\overline{Q}$.

3.3 Truth Table

From the timing chart above (see Fig 4) we get:

S	R	Q
0	0	previous state
0	1	0
1	0	1
1	1	1 (set dominant)

Figure 5: Obtained truth table for the tested digital circuit.

3.4 Answer

From the truth table we can easily conclude that *set* is the dominant input. Active levels of both inputs are zeroes.

4 Description of the fourth task

Task 5

For a flip-flop constructed as cross-coupled NORs draw a timing chart illustrating the behaviour of the device. Basing on the chart determine the dominant input and the active level of both inputs.

4.1 The circuit

I started by connecting a digital circuit on my machine (see Fig 6).

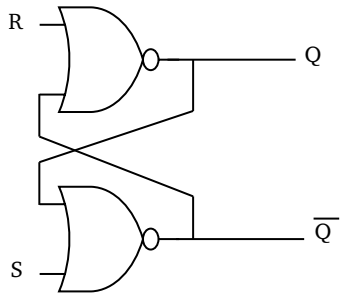

Figure 6: Cross-coupled NOR

After connecting the digital circuit I went to tests to create a timing chart.

4.2 Timing Chart

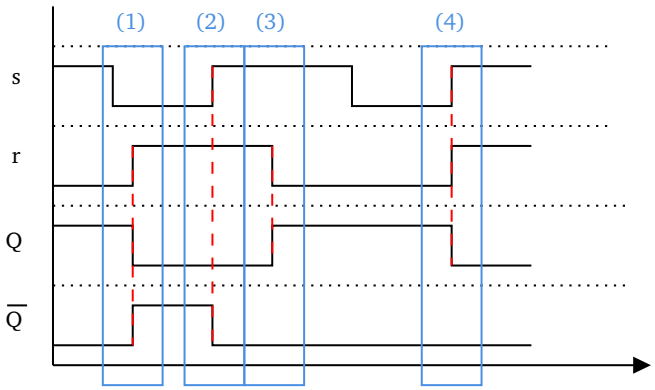

Figure 7: Timing Chart created during laboratory

(1) We can see that r sets Q to 0 and $\overline{Q}$ to 1.

(2) When the r state is high, the s state got changed to high right after. This leads to a change in $\overline{Q}$ from 1 to 0. This way both Q and $\overline{Q}$ are zero.

(3) When r is switched to low, only s is active and the result is $Q = 1$, $\overline{Q} = 0$

(4) When the high state appeared again on two s and r signals at the same time, the result as before is the low state on both outputs.

4.3 Truth Table

Based on the timing chart above (see Fig 4) we get:

S	R	Q
0	0	previous state
0	1	0
1	0	1
1	1	0 (reset dominant)

Figure 8: Obtained truth table for the tested digital circuit.

4.4 Answer

From the truth table we can easily conclude that *reset* is the dominant input. Active levels of both inputs are ones.

5 Conclusions

During the labs, the exercises went exceptionally well. There were no anomalies and calm analysis of the tasks led to correct results. However, one of the main mistakes I made was that I didn't know how to treat on a timing-chart the variables that were negated.