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Electronics and Measurements Laboratory

Ex. 10
Operational Amplifiers

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Exercise performed on 19.10.2020

Purpose of the exercise

The aim of the tasks is to get to know more about the different applications of the operational amplifier. This will result in a better understanding of how they work, as well as an increase in knowledge of their various applications.

1 The inverting amplifier

Task 1

The inverting amplifier. Copy the transfer characteristics and the time waveforms to the lab report. Based on measurements, find the voltage gain, the phase shift and the saturation voltage of the op amp. Discuss the experiment and compare the obtained results with theoretical predictions. Estimate the frequency range in which the output signal is undistorted and explain this phenomenon.

1.1 Static Transfer Characteristics

The static transfer characteristic (see Fig. 2) has been calculated on the basis of the constructed scheme (see Fig. 1). The circut has been set to:

- U_{SET} from -10 V to 10V
- 1 V step

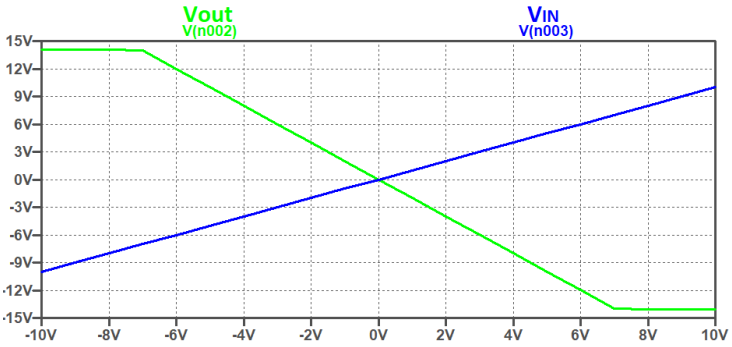


Figure 1: Static Transfer Characteristic

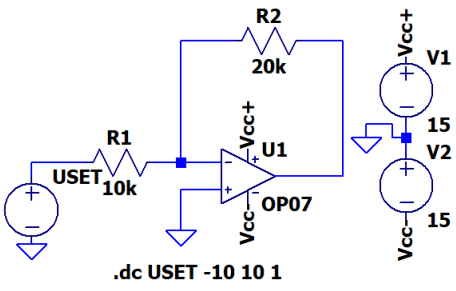


Figure 2: Circuit used for calculations

1.2 Transfer Characteristic

In this circuit the voltage source has been changed to a sinusoidal source.

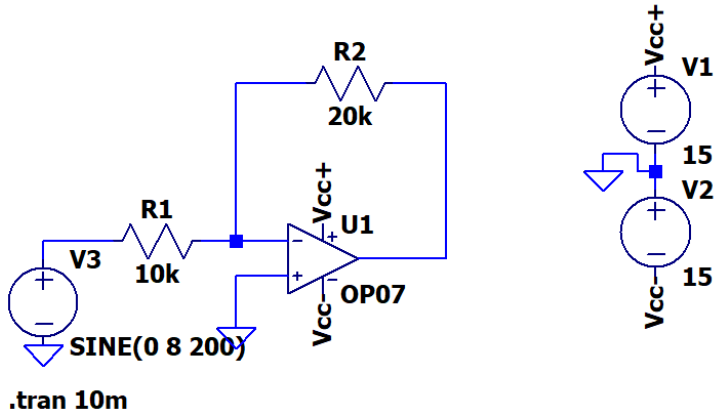


Figure 3: The circuit used for the following calculations.

From the above arrangement we obtain the following graph showing the input and output voltage.

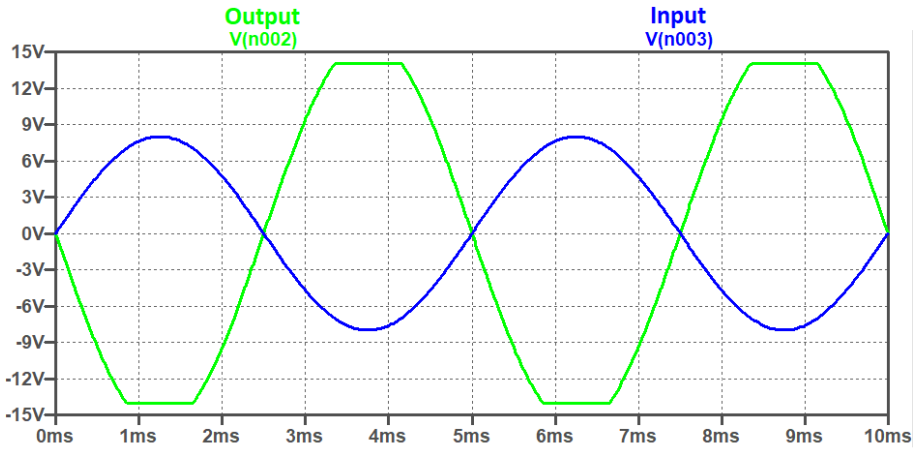


Figure 4: Graph showing the input and output voltage

1.2.1 Phase Shift

The diagram (see Fig. 4) shows very well that the phase shift is 180 degrees - which is not surprising for inverting amplifiers.

1.2.2 Saturation

We can also see immediately the saturation voltage, which is in the graph -14 V and 14 V. We conclude it on the basis of some "flattening" of the sinus - this is the moment when the operational amplifier would like to, but is not able to deliver more voltage to the circuit.

Of course, in a purely theoretical case, where we would have a non-existent ideal operational amplifier, this would not happen. The ideal operational amplifier would not be limited by saturation, as its $U_{VCC-} = -\infty$, and $U_{VCC+} = \infty$. So in this example there would be no problem and it would be able to power up to this 16V (8×2).

1.2.3 Voltage Gain

To obtain the voltage gain I will take the output voltage and divide it by the input voltage. In the graph I also select a point at time t = 2.0092915 ms to calculate the voltage gain. The results are shown in the pictures below.

Point selected at the input

Point selected at the output

$$\text{Voltage Gain } = \frac{-9.2734367\ V}{4.63223096\ V} \approx -2$$

Of course, it is easier to calculate Voltage Gain directly from the circuit, where it would be here:

$$k_u = \frac{u_{out}}{u_{in}} = -\frac{R_2}{R_1}$$

We can use this as some sort of check where it actually is:

$$k_u = \frac{u_{out}}{u_{in}} = -\frac{R_2}{R_1} = -\frac{20\ k\Omega}{10\ k\Omega} = -2$$

We are therefore sure that the result is as correct as possible.

1.2.4 Frequency range in which the output signal is undistorted

For this task, I use the circuit below. I will only gradually increase the frequency in it.

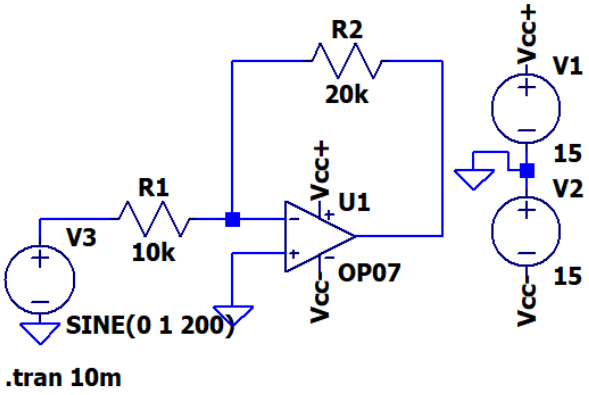


Figure 5: The circuit used for the following calculations.

For example from the above circuit (Fig. 5) (200 Hz) we get the following diagram:

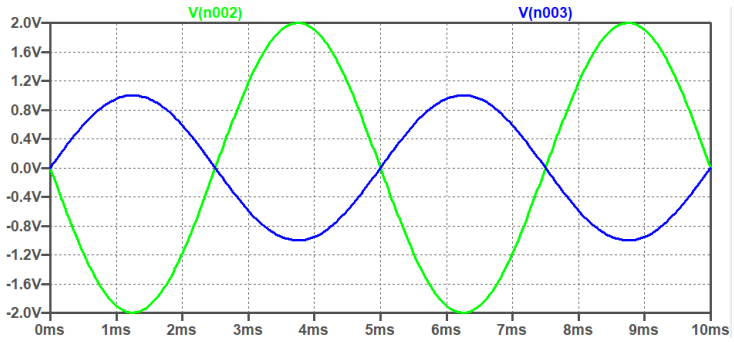
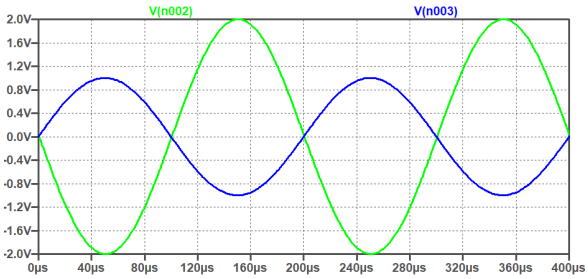
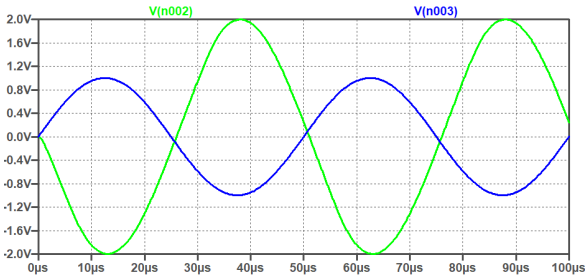


Figure 6: The diagram of the Fig. 5 (200Hz)

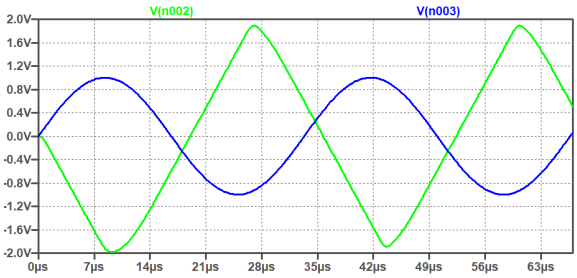
Let's consider some additional graphs for given frequencies: *5000 Hz, 20 000 Hz, 30 000 Hz, 35 000 Hz*



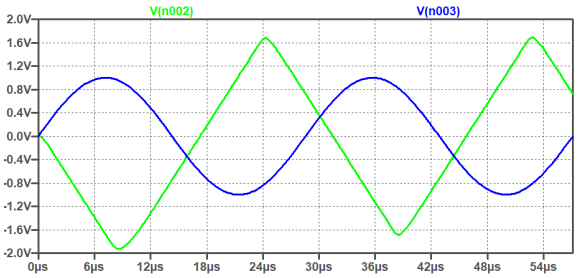
Frequency of 5000 Hz



Frequency of 20 000 Hz



Frequency of 30 000 Hz



Frequency of 35 000 Hz

There is an animated gif how frequency affects the output
https://drive.google.com/uc?export=view&id=1T-jV65-GQqSaoZ55kBRNn5e65H5rz9Uy

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However, we can see that the graph is behaving quite strangely. Over time it seems to get closer together and then it becomes "triangular". Why is this happening? A real amplifier always has some limitations to the ideal one. The distortion shown in the pictures is directly related to the SR (slew rate) parameter.

$$\text{Slew Rate} = \frac{\text{the change of output voltage}}{\text{time at the output when this change occurred}} = \frac{\Delta U_{out}}{\Delta T}$$

Let's do this with an example:

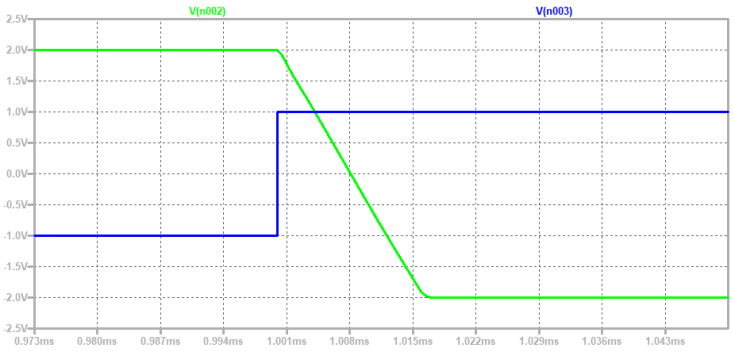


Figure 7: Obtained diagram

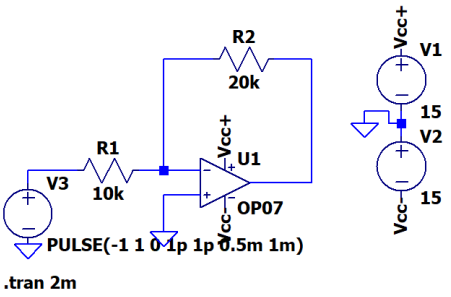


Figure 8: Circuit used for this measurement

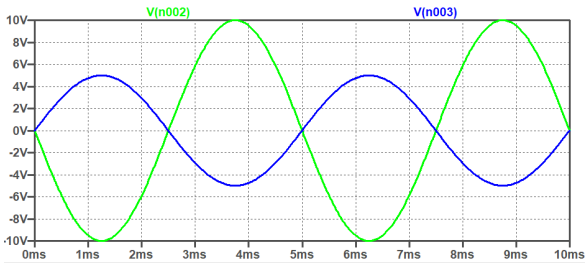
Info: In order to better explain this phenomenon, a slightly different circuit is presented. Setting the source to Pulse allows to get a rectangle that has a period of 1ms (1khz) and filling of 1/2. The settings are supposed to resemble the ideal source. To do that the rising slope and falling slope is set to onepicosecond.

What we see in the diagram (Fig. 7) is a rapidly changing input and an output that cannot catch up with this change. This parameter means – in this example given in the picture (see Fig. 7) – that in 15 ms the voltage is not able to change more than 4V.

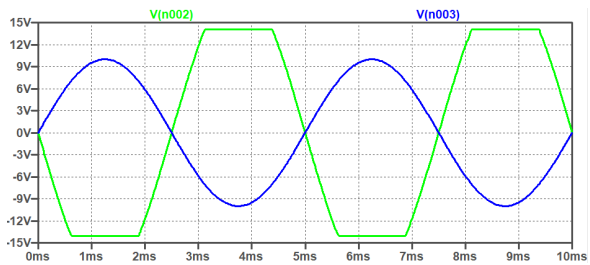
This leads to a "triangular appearance" of our function. The operational amplifier does not keep up with the change, which is greatest where sine values are equal to zero – where the delta is greatest. Because the operational amplifier can't keep up with the change, due to delay it has to turn back and run down before it reaches the peak that the sine function has.

1.2.5 The change of amplitude

In the next exercise at frequency of 200 Hz, I change the amplitude value.



Amplitude of 5 V



Amplitude of 10 V

The specific thing that can occur if the amplitude is too high is the saturation, which has already been explained in **1.2.2. Saturation**.

2 The noninverting amplifier

Since most of these subjects have been explained in quite some detail in section **1. The inverting amplifier** (see page 2), let me shorten this section a little bit without repeating the descriptions, but rather with simple solutions.

Task 2

The noninverting amplifier. Copy the transfer characteristics and the time waveforms to the lab report. Based on measurements, find the voltage gain, the phase shift and the saturation voltage of the op amp. Discuss the experiment and compare the obtained results with theoretical predictions.

2.1 Static Transfer Characteristics

The static transfer characteristic (see Fig. 10) has been calculated on the basis of the constructed scheme (see Fig. 9). The circut has been set to:

- U_{SET} from -10 V to 10V
- 1 V step

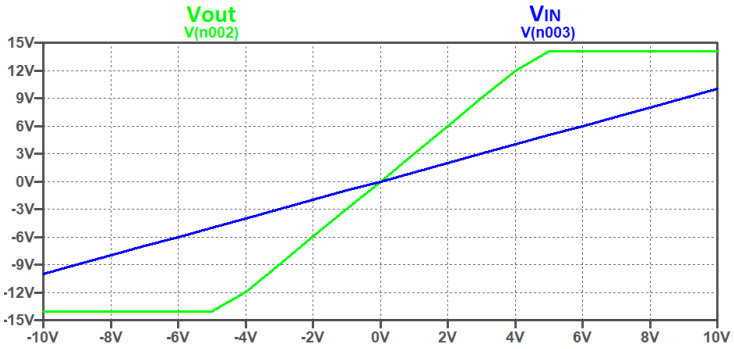


Figure 9: Static Transfer Characteristic

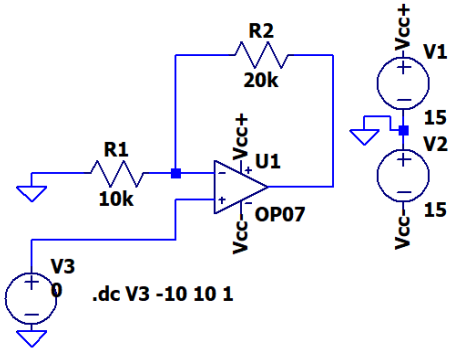


Figure 10: Circuit used for calculations

This space has been intentionally left blank.

2.2 Time waveforms

A (almost) new circuit was built for the calculations below. The voltage source has been changed to a sinusoidal source.

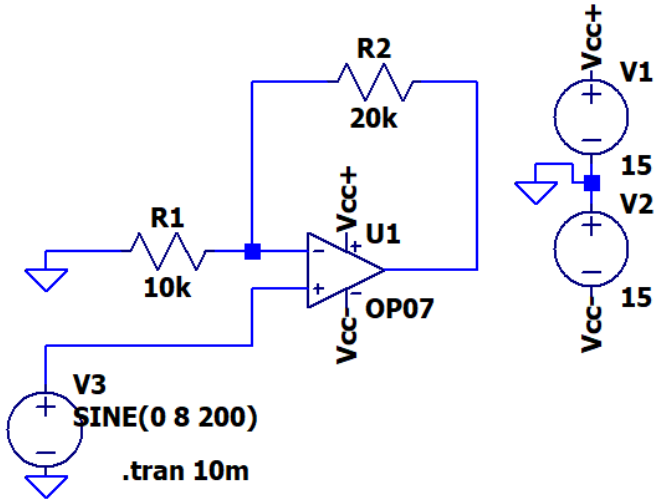


Figure 11: The circuit used for the following calculations.

From the above arrangement we obtain the following graph showing the input and output voltage.

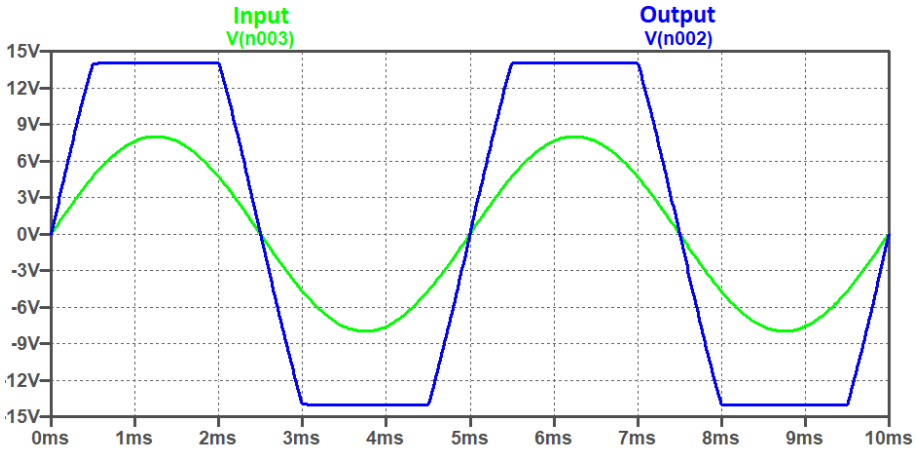


Figure 12: Graph showing the input and output voltage

2.2.1 Phase Shift

The diagram (see Fig. 12) shows very well that there is no phase shift (is in phase) - which is not surprising for noninverting amplifiers.

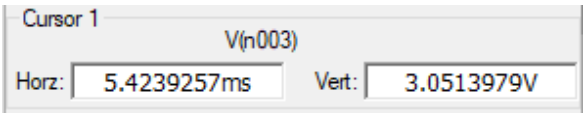
2.2.2 Saturation

We can also see immediately the saturation voltage, which is -14 V and 14 V. We conclude it on the basis of some "flattening" of the sinus - this is the moment when the operational amplifier would like to, but is not able to deliver more voltage to the circuit.

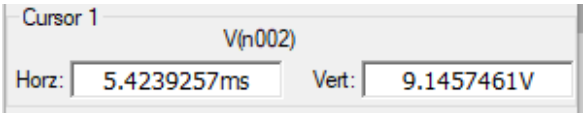
Of course, in a purely theoretical case, where we would have a non-existent ideal operational amplifier, this would not happen. The ideal operational amplifier would not be limited by saturation, as its $U_{VCC-} = -\infty$, and $U_{VCC+} = \infty$. It would be able to power up to 18V (8×3) if only it would be an ideal component.

2.2.3 Voltage Gain

To obtain the voltage gain I will take the output voltage and divide it by the input voltage. In the graph I also select a point at time t = 5.4239257 ms to calculate the voltage gain. The results are shown in the pictures below.



Point selected at the input



Point selected at the output

$$\text{Voltage Gain } = \frac{9.1457461\ V}{3.0513979\ V} \approx\ 3$$

Of course, it is easier to calculate Voltage Gain directly from the system, where it would be here:

$$k_u = \frac{u_{out}}{u_{in}} = 1 + \frac{R_2}{R_1}$$

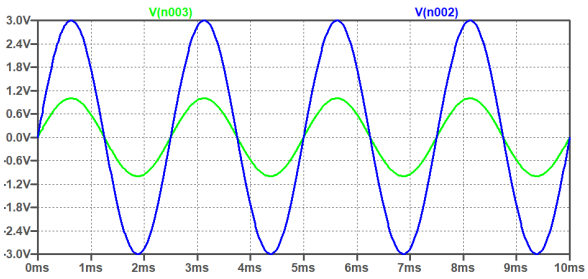
We can use this as some sort of check where it actually is:

$$k_u = \frac{u_{out}}{u_{in}} = 1 + \frac{R_2}{R_1} = 1 + \frac{20\ k\Omega}{10\ k\Omega} = 3$$

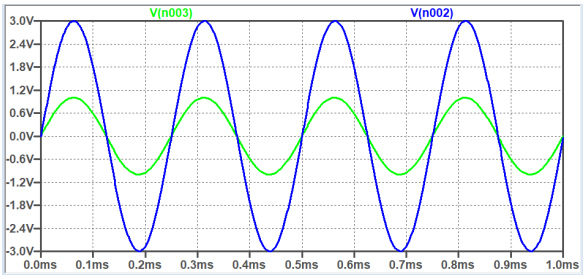
We are therefore sure that the result is as correct as possible.

2.2.4 Other measurements

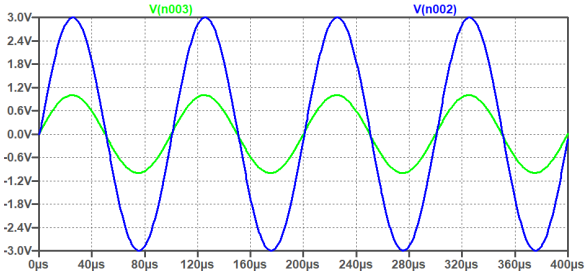
There were also exercises connected with increasing the amplitude and frequency. In the first exercise for 1 V amplitude I change the frequency value.



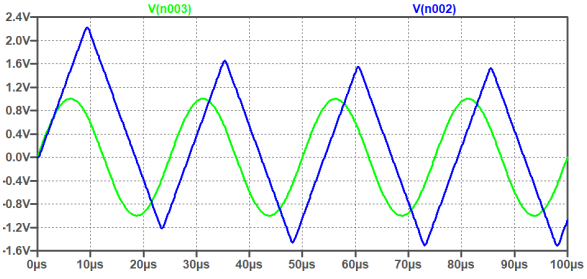
Frequency of 400 Hz



Frequency of 4000 Hz



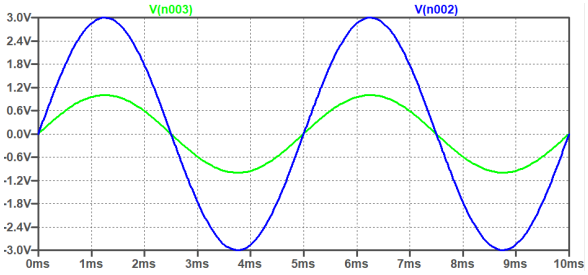
Frequency of 10 000 Hz



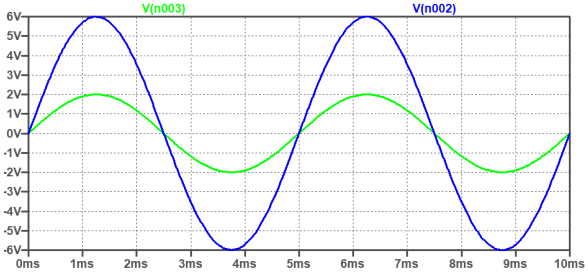
Frequency of 40 000 Hz

Here, however, no surprise. We see how, at some point, the changes at the input happen too quickly for the operational amplifier to keep up with them. However, I see no reason to discuss this phenomenon again, as it has already been discussed on page 4 in section **1.2.4. Frequency range in which the output signal is undistorted**.

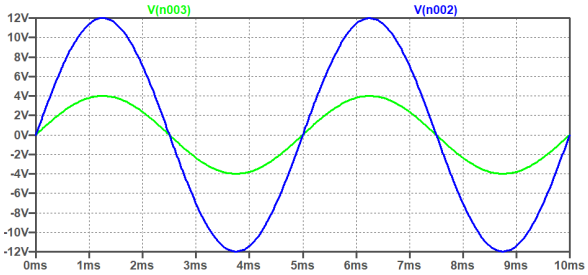
In the next exercise at frequency of 200 Hz, I change the amplitude value.



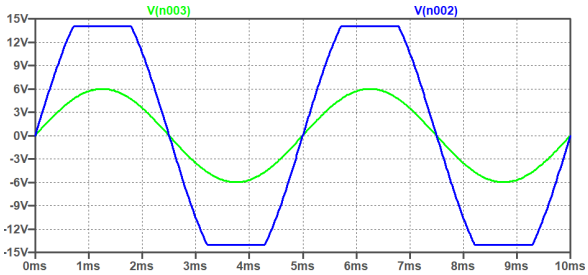
Amplitude of 1 V



Amplitude of 2 V



Amplitude of 4 V



Amplitude of 6 V

Here, as before, when we increase the amplitude at the input of the circuit, at some point the operational amplifier wants to amplify the signal far too much beyond its capabilities. Therefore, we see the sinus gradually flattening out. This was also discussed on page 3 in section **1.2.2. Saturation**.

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3 The differential amplifier

Task 3

The differential amplifier. Copy the transfer characteristics to the lab report. Based on characteristics, determine the differential mode voltage gain and the common-mode voltage gain. Calculate the CMRR. Discuss the obtained results

3.1 Transfer Characteristics for Differential Mode

For both diagrams this circuit was used. The only difference is the u_c value. Here it is 0 V, but it was changed to 5V in further calculations. Let me not duplicate pictures of this circuit twice.

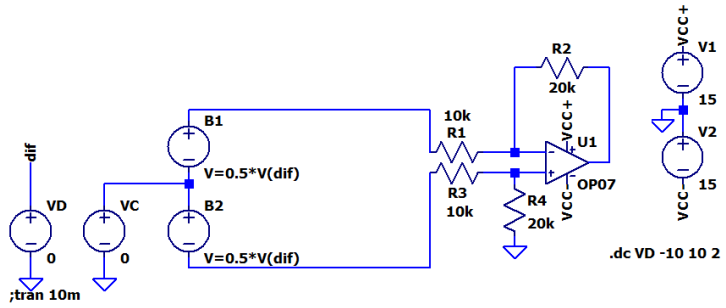


Figure 13: The circuit used for the following calculations.

3.1.1 Transfer Characteristics for u_c = 0V

The transfer characteristic (see Fig. 14) has been calculated on the basis of the constructed scheme (see Fig. 13). The circut has been set to:

- u_c = 0 V
- u_d from -10 V to 10 V
- 2 V step

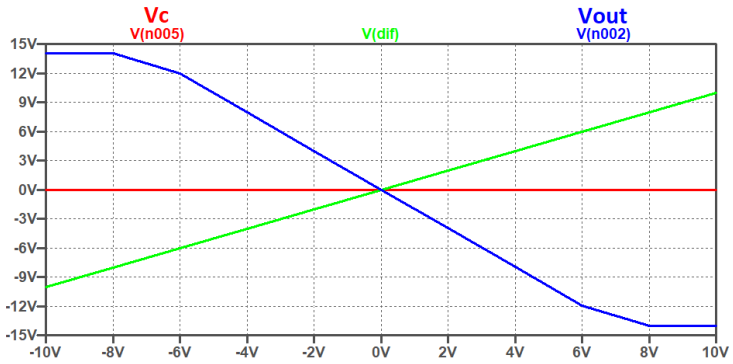


Figure 14: The obtained transfer characteristic for u_c = 0 V

It is immediately apparent that the value is not only enhanced, but also reversed. We will calculate the voltage gain in **3.1.3. Differential Mode Voltage Gain**.

3.1.2 Transfer Characteristics for u_c = 5 V

The circut has been set to:

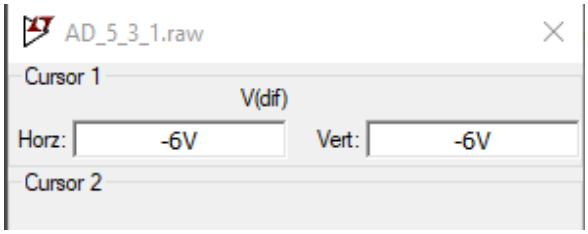
- u_c = 5 V
- u_d from -10 V to 1 0V
- 2 V step

Figure 15: The obtained transfer characteristic for u_c = 5 V

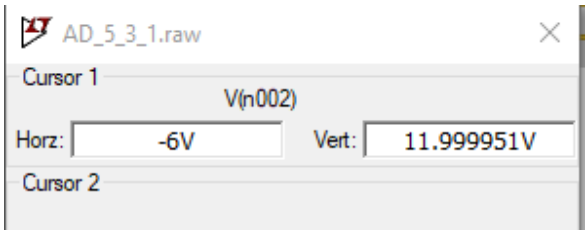
As we can see, compared to the results for u_c = 0 V (section 3.1.1), they are even identical. This means that the interference... maybe not that they do not affect the signal at all, more like it hardly affects the output signal (as we are not dealing with an ideal component).

3.1.3 Differential Mode Voltage Gain

It should not make much difference which of the two charts we take the data from. We choose two points – one for the V_{diff} and the other for the V_{out} chart. Both should be on the same point of V_d axis.



Point selected at the V_{diff}



Point selected at the V_{out}

$$\text{Voltage Gain} = \frac{V_{out}}{V_{diff}} = \frac{11.999951\ V}{-6\ V} \approx -2$$

Of course, it is easier to calculate Voltage Gain directly from the circuit, where it would be here:

$$k_u = -\frac{R_2}{R_1}$$

We can use this as some sort of check where it actually is:

$$k_u = -\frac{R_2}{R_1} = -\frac{20\ k\Omega}{10\ k\Omega} = -2 \tag{1}$$

We are therefore sure that the result is as correct as possible.

3.2 Transfer Characteristics for Common-Mode

The circuit is the same, although we will now increase the noise value u_c, and the V_{diff} is now turned off.

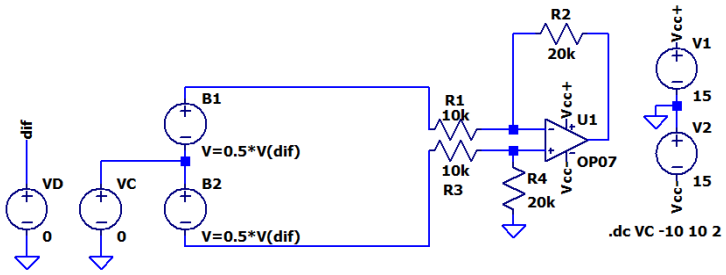


Figure 16: The circuit used for the following calculations.

The circut has been set to:

- u_d = 0 V
- u_c from -10 V to 10 V
- 2 V step

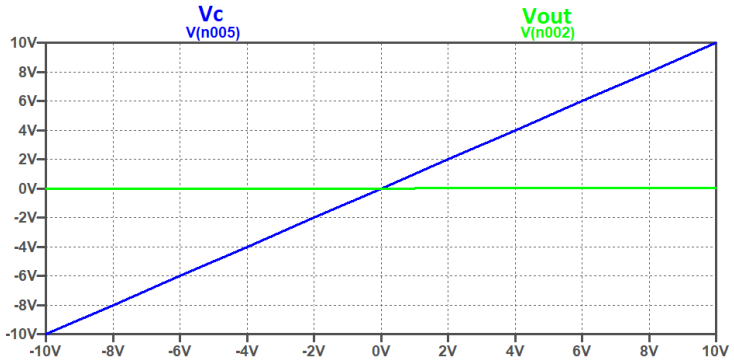
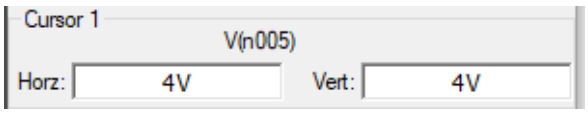


Figure 17: The obtained transfer characteristic for u_c = 0 V

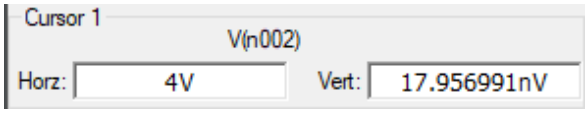
It would seem that our differential amplifier does not amplify the noise signal at all and the output is pure zero. Unfortunately, it is not! Our differential amplifier is not perfect and amplifies the noise signal, although it is close to zero. We will see this on the selected points to calculate the Voltage Gain in the section **3.2.1. Common-Mode Voltage Gain**.

3.2.1 Common-Mode Voltage Gain

It should not make much difference which of the two charts we take the data from. We choose two points – one for the V_c and the other for the V_{out} chart. Both should be on the same point of V_c axis.



Point selected at the V_c



Point selected at the V_{out}

$$\text{Voltage Gain} = \frac{V_{out}}{V_c} = \frac{17.956991\ nV}{4\ V} = 4.489248 \times 10^{-9} \approx 0 \tag{2}$$

The result obtained is so small that it is irrelevant. We can say that the reinforcement is close to zero. Another way to calculate this, of course, was to take two points on the V_{out} and examine their slope. The result would be the same.

3.3 CMRR

Using the calculated *Differential Voltage Gain* (equation 1 on page 12) and *Common-Mode Voltage Gain* (equation 2 on page 12) we have:

$$CMRR = \frac{|k_D|}{|k_{CM}|} = \frac{2}{4.489248 \times 10^{-9}} \approx 4.455089 \times 10^{8}$$

This space has been intentionally left blank.

4 The summing amplifier

Task 4

The summing amplifier. Determine the function $U_{out} = f(U_{SET}, e_g)$ (the values of the resistors are given in section 5.4). Copy the output waveforms to the lab report. Based on obtained waveforms, find the analytical expression for U_{out} and compare with theoretical relation.

4.1 The diagram of function $U_{out} = f(U_{SET}, e_g)$

The first task was to build a circuit whose U_{SET} would be zero. Generator e_g should produce sinus function with frequency 200Hz and with amplitude 3 V.

Warning: This circuit will also be used for different U_{SET} values. However, I won't paste it more times for this reason. Please take this into account.

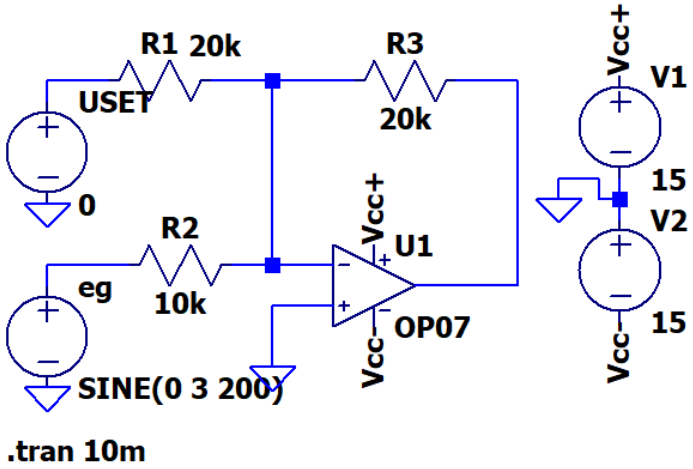


Figure 18: The circuit used for the following calculations.

From the above circuit (see Fig. 18) we get the diagram below (see Fig. 19). We can see that the output amplitude has been properly amplified twice (and its phase shift is 180 degrees) - so the amplifier itself works properly.

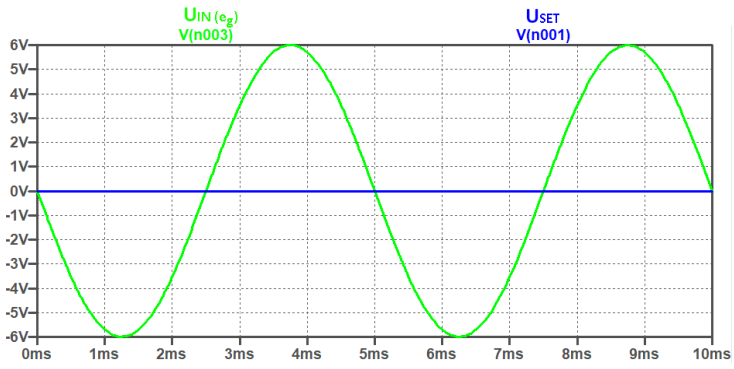


Figure 19: The circuit used for the following calculations.

Nothing special is happening at this point, so let's move forward and start changing U_{SET}.

4.1.1 Diagrams for different values of U_{SET}

True magic starts to happen with a U_{SET} value change.

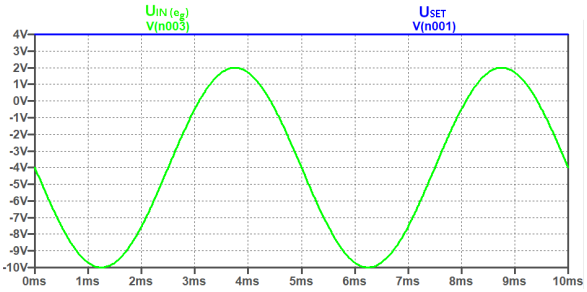


Diagram for U_{SET} = 4 V

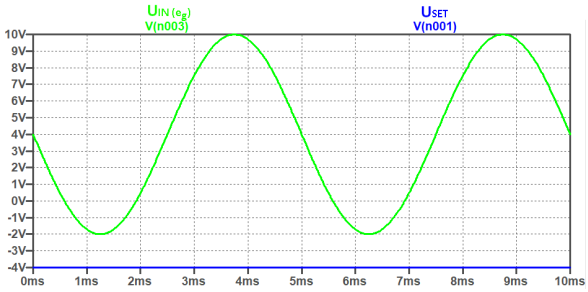


Diagram for U_{SET} = -4 V

What we can already see is that changing the U_{SET} value shifts our sinus function up or down. What does this mean? It means that it is a circuit that sums up signals from two sources. In this case it is the sum of our U_{SET} and our e_g.

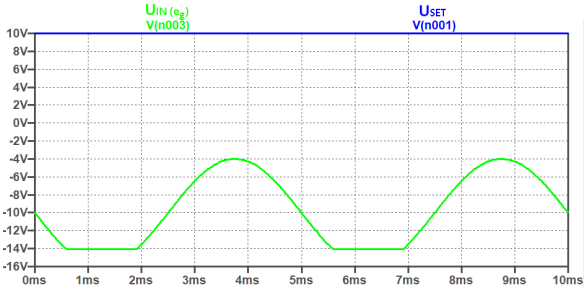


Diagram for U_{SET} = 10 V

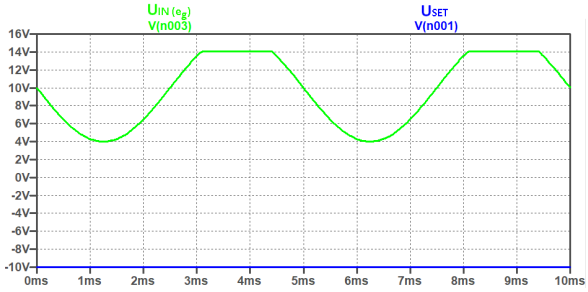


Diagram for U_{SET} = -10 V

One might ask: *Ahaa! If this digital circuit only sums up what it has done to me with this graph for U_{SET} = 10 V and -10 V? It doesn't look like a sum to me at all!*

But it is still the sum, except that we don't operate on ideal components, so we are limited by V_{SAT+} and V_{SAT-} of our summation amplifier. Here we see that it will not work miracles and will not bypass its own limitations, so in this case it cannot amplify this value to more than the 14V and -14V shown in the given charts.

4.1.2 Analytical expression for U_{out}

Using the superposition principle we first calculate U_{out} for the U_{SET} turned off:

$$U_{out_1} = e_g(t) \times \left(-\frac{R_3}{R_2}\right)$$

And then for the e_g off.

$$U_{out_2} = U_{SET} \times \left(-\frac{R_3}{R_1}\right)$$

The superposition rule gives an expression:

$$U_{out} = e_g(t) \times \left(-\frac{R_3}{R_2}\right) \; + \; U_{SET} \times \left(-\frac{R_3}{R_1}\right)$$

Then for our circuit:

$$U_{out} = e_g(t) \times (-2) \; + \; U_{SET} \times (-1) = -2\, e_g(t) \; - \; U_{SET}$$

5 The voltage comparator

Task 5

The voltage comparator. Copy the transfer characteristics to the lab report. Compare obtained characteristics with a theoretical predictions

5.1 Transfer Characteristic

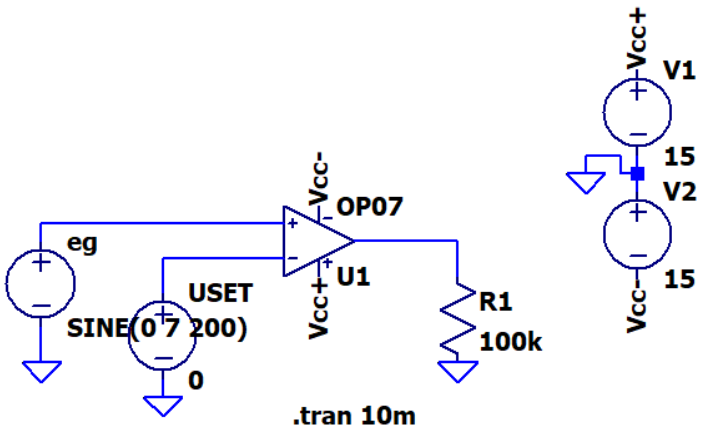


Figure 20: The circuit used for the following calculations.

For the above voltage comparator we obtain the following characteristics:

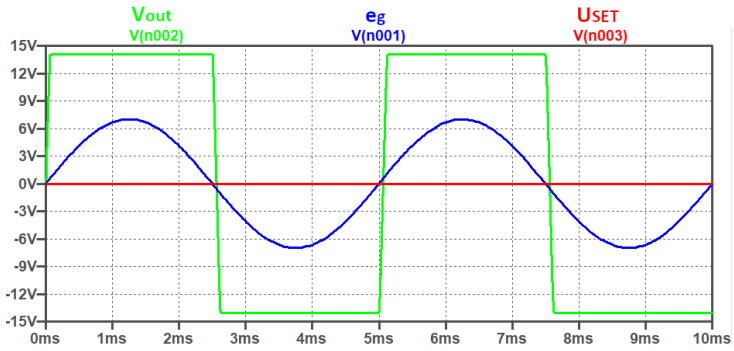


Figure 21: Diagram for the $U_{SET} = 0$

What we can see is that at the output comparator gives its V_{SAT+} when the value of e_g is greater than the value of U_{SET}. If the value of e_g is less than the value of U_{SET} then at the output we get the value of V_{SAT-} of the voltage comparator.

$$e_g > U_{SET} \longrightarrow U_{OUT} = V_{SAT+}$$
$$e_g < U_{SET} \longrightarrow U_{OUT} = V_{SAT-}$$

Now let's change the U_{SET} a little.

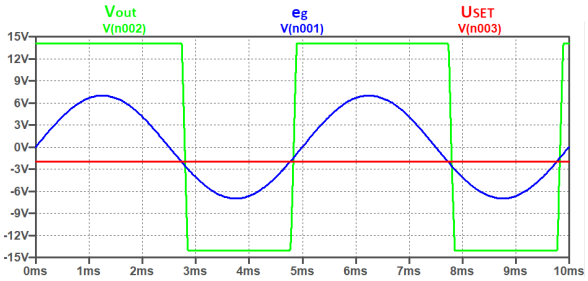


Diagram for U_{SET} = -2

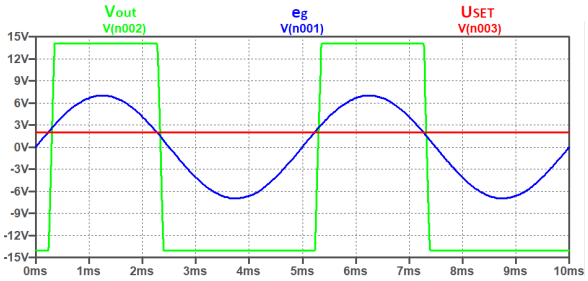


Diagram for U_{SET} = 2

As we can see, the circuit is behaving in accordance with our assumptions.

6 The voltage comparator with hysteresis

$$REMOVED... \; sorry \; ; w;$$

7 Conclusions

Operating amplifiers are not as simple components as they might seem. It may not be as difficult to use them, but it is probably not easy to fully understand them. Tasks with them are easy to complicate. Just as they didn't seem difficult during the lectures, it wasn't easy to get into contact with them for the first time. This has taught me a lot and I will probably learn even more from my mistakes.