Digital Circuits Theory - Laboratory						
Academic year	Laboratory exercises on	Mode of studies	Field of studies	Supervisor	Group	Section
2020/2021	Wednesday 16:30 – 18:15	SSI	Informatics	KP	1	3

Report from Exercise No 5

Performed on: 14.10.2020

Exercise Topic: Synchronous Sequential Circuits

Performed by:

Dawid Grobert

Purpose of the exercises

The aim of the exercises was to get familiar with the synchronous sequential circuits in practice by solving the given tasks and to test them on the machines by oneself.

1 Description of the first task

Task 1

Design a synchronous sequential circuit detecting odd number of logic 1s in 2-bit words sent to the serial input X. Detection should cause the output to become set for the time not longer than one clock period.

I assume that the first bit is LSB. In simpler words, in case of 2-bit words it means that the output should show 1 for inputs 01 and 10, and 0 for inputs 00 and 11.
For example:

```
Input:  00|01|11|10 ⟵ Staring from LSB
Output: 00|10|00|10
```

1.1 State Diagram

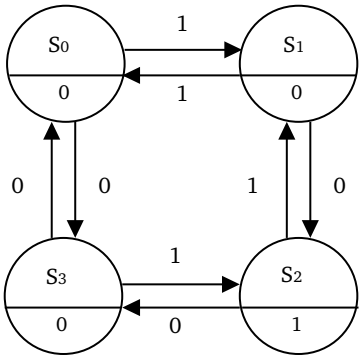


Figure 1: State diagram made during laboratories

1.2 Implementation

I start with the state assignment:

Present state	P: 0	P: 1	Z
S_0	S_3	S_1	0
S_1	S_2	S_0	0
S_2	S_3	S_1	1
S_3	S_0	S_2	0

Next state

$Q_1^t Q_0^t$	P: 0	P: 1	Z
00	10	01	0
01	11	00	0
11	10	01	1
10	00	11	0

Q_1^{t+1} Q_0^{t+1}

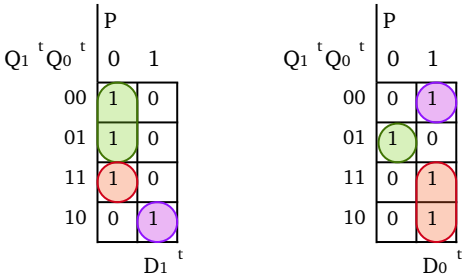
$S_0 = 00$

$S_1 = 01$

$S_2 = 11$

$S_3 = 10$

Then I prepare two Karnaugh Maps for Flip-Flops D:



From given maps I get:

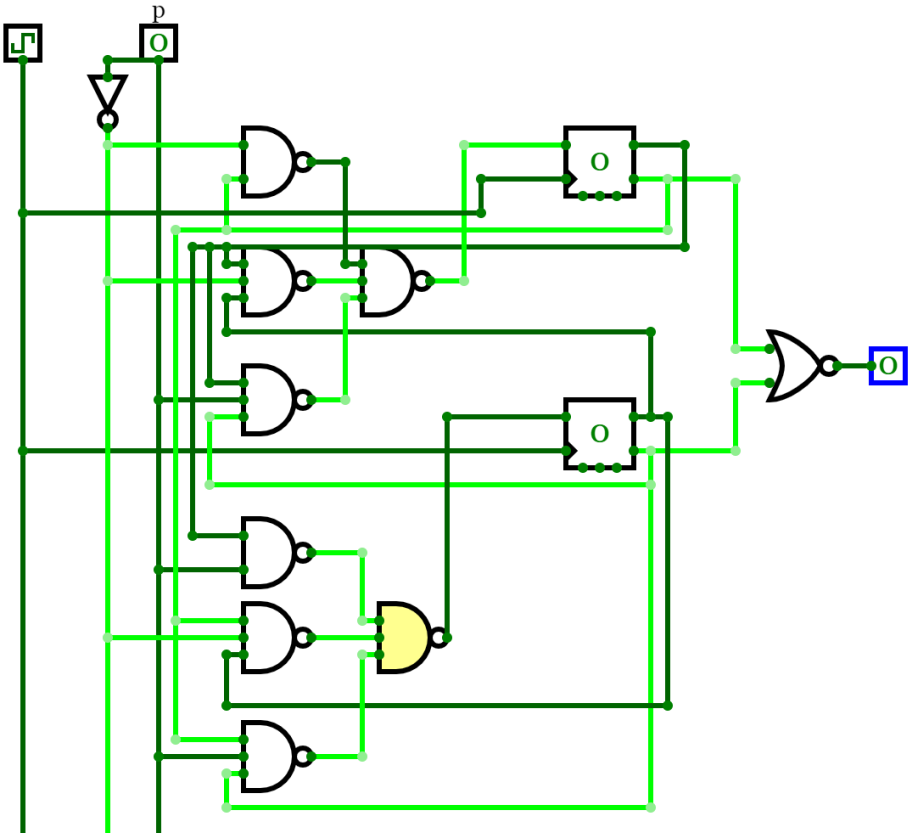
$$D_1^t = \overline{\overline{\overline{Q_1^t}\,\overline{p}} \times \overline{Q_1^t\,Q_0^t\,\overline{p}} \times \overline{Q_1^t\,\overline{Q_0^t}\,p}}$$

$$D_0^t = \overline{\overline{Q_1^t\,p} \times \overline{\overline{Q_1^t}\,Q_0^t\,\overline{p}} \times \overline{\overline{Q_1^t}\,\overline{Q_0^t}\,p}}$$

And the output function is:

$$W = Q_1^t Q_0^t = \overline{\overline{Q_1^t} + \overline{Q_o^t}}$$

1.3 Circuit simulation



2 Description of the second task

Task 7

Design a synchronous circuit executing operation of multiplication by 2 of N-bit binary number, sent to the serial input X starting from the least significant position.

In simpler terms, the circuit should output sequences of numbers from the input, but with an additional zero added first.
For example:

```
Input:  101110111 ⟵ Staring from LSB
Output: 1011101110
```

2.1 State Diagram

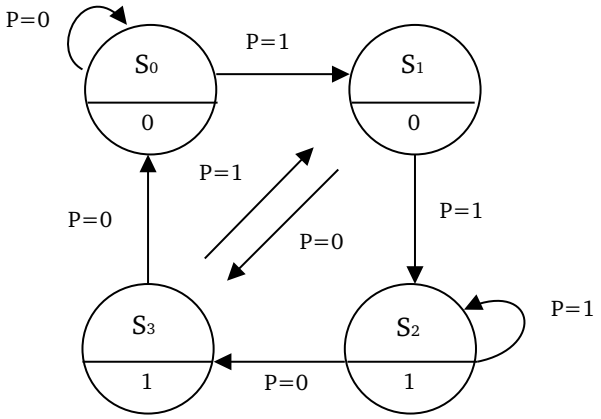


Figure 2: State diagram made during laboratories

2.2 Implementation

I start with the state assignment:

Present state	P = 0	P = 1	Z
S_0	S_0	S_1	0
S_1	S_3	S_2	0
S_2	S_3	S_2	1
S_3	S_0	S_1	1

Next state

$Q_1{}^tQ_0{}^t$	P = 0	P = 1	Z
00	00	01	0
01	10	11	0
11	10	11	1
10	00	01	1

$Q_1{}^{t+1}Q_0{}^{t+1}$

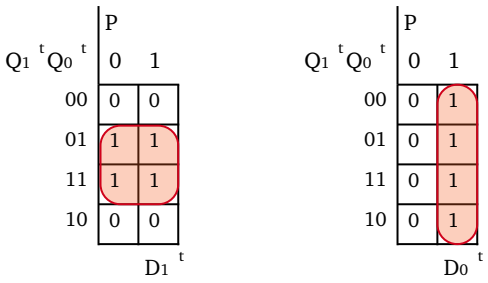
$S_0 = 00$

$S_1 = 01$

$S_2 = 11$

$S_3 = 10$

Then I prepare two Karnaugh Maps for Flip-Flops D:



From given maps I get:

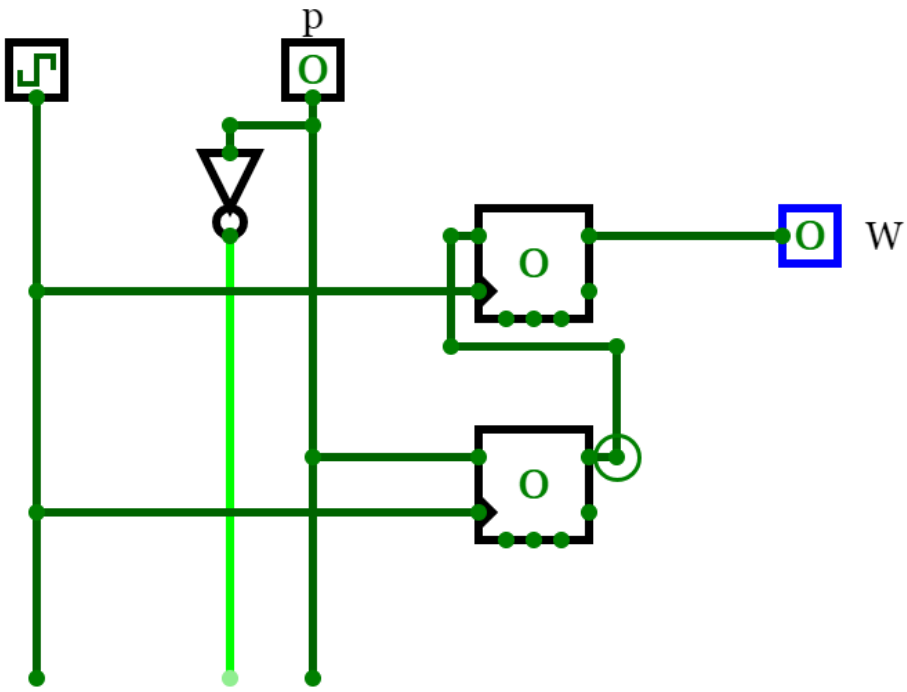
$D_1^t = Q_0^t$

$D_0^t = p$

The output function is:

$W = Q_1^t$

2.3 Circuit simulation



3 Description of the third task

Task 3

Design a synchronous sequential circuit detecting than a binary 2-bit number corresponding to the 2-bit words sent to the serial input X, is an odd number. The first bit of the word is assumed to be LSB. Detection should cause the output to become set for the time not longer than one clock period.

In other words, the task is to check whether the first bit given is one or zero. If it is a one, it means that the number given is an odd number – so it should display one in two subsequent clock cycles as information about the oddity of the number.

If the first bit is zero, it will display zero (as the given number is even) for two cycles of the clock. Every second number given we checked for evenness/oddity of the whole two-bit number.

For example:

```
Input:  00|01|11|10 ⟵ Staring from LSB
Output: 00|11|11|00
```

3.1 State Diagram

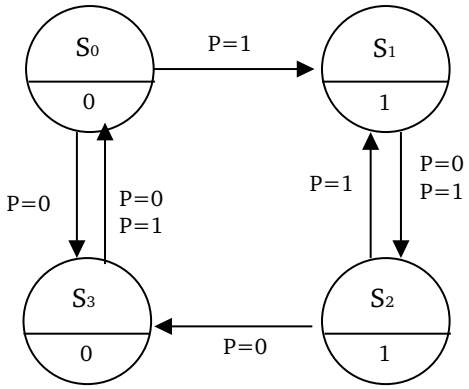


Figure 3: State diagram made during laboratories

3.2 Implementation

I start with the state assignment:

Present state	P = 0	P = 1	Z
S_0	S_3	S_1	0
S_1	S_2	S_2	1
S_2	S_3	S_1	1
S_3	S_0	S_0	0

Next state

$Q_1^t Q_0^t$	P = 0	P = 1	Z
00	10	01	0
01	11	11	1
11	10	01	1
10	00	00	0

$Q_1^{t+1} Q_0^{t+1}$

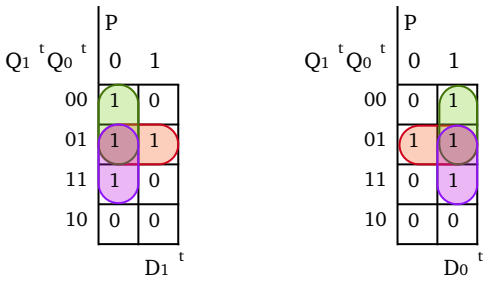
$S_0 = 00$

$S_1 = 01$

$S_2 = 11$

$S_3 = 10$

Then I prepare two Karnaugh Maps for Flip-Flops D:



From given maps I get:

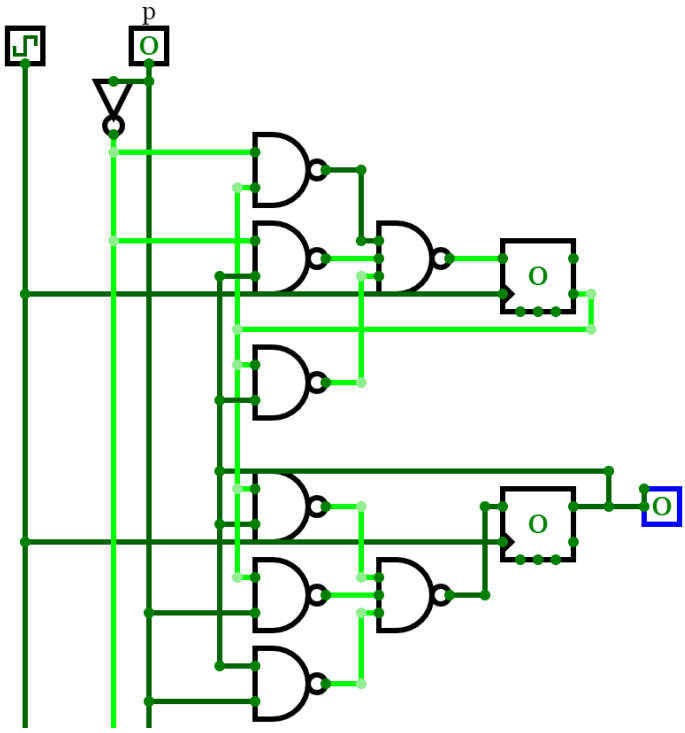
$D_1^t = \overline{p}\,\overline{Q_1^t} + \overline{p}\,Q_0^t + \overline{Q_1^t}Q_0^t = \overline{\overline{\overline{p}\,\overline{Q_1^t}} \times \overline{\overline{p}\,Q_0^t} \times \overline{\overline{Q_1^t}Q_0^t}}$

$D_0^t = \overline{\overline{\overline{Q_1^t}\,Q_0^t} \times \overline{\overline{Q_1^t}\,p} \times \overline{Q_0^t\,p}}$

The output function is:

$W = Q_0^t$

3.3 Circuit simulation



4 Conclusions

During the labs, many tasks were initially carried out incorrectly and had to be corrected on the spot. A clear connection of gates and cables helped a lot in the implementations. This allowed the connection of the system to be reconsidered in case of problems instead of building it from the beginning.

One of the mistakes I made was in "Task 1". Initially prepared diagram had states, which in subsequent states led to themselves. Such a diagram at that point "forgot" to which bit it points. Consequently, it did not know whether it was pointing to MSB of a two-bit word or the LSB.

I also made a mistake in "Task 3", where initially I displayed information about odd numbers only for one clock.